REMARKS/ARGUMENTS

Claims 1-44 were originally presented.

Claims 1, 6-9, 16, 23, 33, and 42-44 are previously presented.

No claims are currently amended

No claims are canceled.

Claims 1-44 remain in this application.

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,799,168 to Ban (hereinafter "Ban").

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,000,006 to Bruce *et al.* (hereinafter "Bruce").

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,493,807 to Martwick (hereinafter "Martwick").

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,253,281 to Hall *et al.* (hereinafter "Hall").

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall and further in view of Bruce.

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall, further in view of Martwick.

Claims 1-44 remain in this application.

Telephone Conversation with Examiner

Applicant wishes to thank the Examiner for the telephonic conversation on March 7, 2006. In particular Applicant appreciates the Examiner's provisional acceptance of the arguments included below regarding the 35 U.S.C. §102 rejections.

35 U.S.C. §102(b)

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected under 35 U.S.C. §102(b) as being anticipated by Ban. Applicant respectfully traverses the rejection.

Independent claim 1 recites:

> One or more computer-readable media comprising a flash memory driver that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising:
>
> flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media; and
>
> flash media logic configured to interact with different types of the flash memory media;
>
> wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media, and further wherein the flash memory driver is flash memory medium agnostic.

Ban fails to disclose the one or more computer-readable media comprising a flash memory driver of claim 1. Rather, Ban discloses shifting the responsibility for conforming to the particular requirements of a flash chip from a standardized

driver installed on a CPU to a controller *installed on a flash unit.* (Ban, Col. 2, lines 36-38 and 42-46). The standardized driver on the CPU sends out commands necessary to perform flash memory tasks in a uniform, standardized format. (Ban Col. 2, lines 36-38 and 42-43). The standardized commands (read, write, erase and identify) are received via a command register and are translated by the standardized controller *on the flash unit* (through a translating apparatus) into commands specific to the type of flash chip on which the controller is installed. (Ban, Col. 3, lines 1-15 and Col. 5, lines 29-33). Thus, when a flash array including multiple flash chips is used, each flash chip must be provided with a standardized controller customized to interact with only the particular chip *to which it is attached.* (Ban, Col. 4, lines 33-35, claim 2 lines 29-30). Consequently, in order for the CPU to communicate with several different types of flash chips, a corresponding number of different, uniquely customized controllers must be utilized on each flash chip.

Moreover, the possible output from the CPU is limited to standardized signals. (Ban, Col. 2, lines 41-47). Thus multiple file systems having multiple signal types may not be used under Ban.

As a result, Ban fails to disclose "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1. Rather, under Ban the responsibility for conforming to the requirements of a particular flash chip is given to a uniquely configured standardized controller installed on each particular flash chip. Thus, the controllers disclosed by Ban are flash chip specific, and cannot be used with other types of flash chips. Therefore, each time a new flash chip is used, a new type of standardized controller that is compatible with the new flash chip

must be located on the flash chip. Because of this, the controllers disclosed in Ban are ill-equipped "to interact with different types of the flash memory media" as recited in claim 1.

Ban also fails to disclose "flash media logic configured to interact with different types of the flash memory media". As noted above, the controllers disclosed in Ban are flash chip specific. Thus no one controller could interact with several different types of flash chips. Under Ban, such functionality could only be attained by employing a plurality of different controllers – with each flash chip requiring its own distinct type of controller.

Moreover, Ban fails to disclose "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Rather, under Ban the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip only.

Additionally, Ban fails to disclose "wherein the flash memory driver is flash memory medium agnostic". Rather, as noted above, under Ban each standardized controller is bound to a particular flash chip and thus is limited to performing memory operations specific to that flash chip only.

In rejecting claim 1, the Office relies on Fig.1, and Col. 2, lines 36-38, Col. 4, lines 33-39 as disclosing a flash memory driver (a controller or group of controllers in Ban) comprising flash abstraction logic invokable by a file system to manage flash memory operations without regard to the type of the one or more flash memory media. (*Office Action*, Page 3). Applicant respectfully disagrees. As noted above, controllers, as disclosed in Ban, are flash chip specific, and cannot be used with more than one type of flash chip. Thus any controller disclosed in

Ban would only be able to manage flash operations with regard to one specific type of chip, and not "without regard to the type of the one or more flash memory media" as recited in claim 1.

The Office also relies on claim 2; the Abstract; Col. 2, lines 36-48; and Col. 4, lines 33-39 and 61-65, of Ban as disclosing flash media logic configured to interact with different types of flash memory media (flash chips); wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media. (*Office Action*, Page 3).

Again, Applicant respectfully disagrees. Since the controllers taught in Ban are flash chip specific, no one controller could interact with different types of flash memory media or perform memory operations that are potentially performed in different ways depending on the type of flash memory media. Rather, such versatile functionality could only be realized through the utilization of a plurality of different controllers, with each controller corresponding to a different type of flash memory media.

Similarly, the Office also relies on Fig. 2 of Ban as disclosing the flash memory driver as being flash memory medium agnostic, and as being located remotely from the flash memory medium (i.e. the flash array in Fig. 1). (*Office Action*, Page 3). Again, Applicant respectfully disagrees. Since the controllers taught in Ban are flash chip specific, no one controller could interact with different types of flash memory media or perform memory operations that are potentially performed in different ways depending on the type of flash memory media. Moreover, Ban discloses that each controller is located on the chip it serves.

Therefore, each controller can only serve one flash chip and each controller cannot be located remotely from the flash chip it serves.

Accordingly, since Ban does not teach all of the elements of claim 1, the §102(b) anticipation rejection of claim 1 based on Ban is not supported. Applicant therefore respectfully requests that the §102(b) rejection of claim 1 be withdrawn.

Dependent claims 5-7 are allowable at the least by virtue of their dependency on base claim 1, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 5-7 be withdrawn.

Independent claim 9 recites:

> A flash driver, comprising:
>
> flash abstraction logic, interposed between a file system and a flash memory medium, configured to:
>
> (a) map a logical sector status from the file system to a physical sector status of the flash memory medium; and
>
> (b) maintain memory requirements associated with operating the flash memory medium;
>
> wherein the flash driver is located remote from the flash memory medium.

Ban fails to disclose the flash driver of claim 9. In particular, as discussed more fully above in conjunction with claim 1, under Ban, each controller is customized for use with a specific flash chip and is necessarily located on the flash chip it serves. This is the opposite of "wherein the flash driver is located remote from the flash memory medium" as recited in claim 9.

In rejecting claim 9, the Office relies on the same bases used in the rejection of claim 1, namely Fig.1; claim 2; the Abstract; Col. 2, lines 36-48; and

Col. 4, lines 33-39 and 61-65 of Ban. (*Office Action*, Page 5). However, the elements of claim 9 are neither disclosed in the cited passages nor anywhere else within Ban. As discussed more fully above, each controller is customized for use with a specific flash chip and is necessarily located on the flash chip it serves. Thus the controllers cannot be located remote from the flash memory medium.

Accordingly, since Ban fails to show each and every element of claim 9 the §102(b) rejection of claim 9 based on Ban is not supported. Applicant therefore respectfully requests that the §102(b) rejection of claim 9 be withdrawn.

Dependent claims 10-11 are allowable due to their dependence from an allowable base claim. These claims are also allowable for their own recited features that, in combination with those recited in claim 9, are neither disclosed nor shown in Ban. Applicant therefore respectfully requests that the §102(b) rejection of claims 10 and 11 be withdrawn.

Independent claim 16 recites:

> A flash driver, comprising:
>
> user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium; and
>
> flash abstraction logic, interposed between a file system and flash memory medium to maintain universal requirements for the operation of the flash memory medium;
>
> wherein the flash memory driver is flash memory medium agnostic.

Ban fails to disclose the flash driver of claim 16. Rather, as discussed in more detail above, Ban teaches the use of flash chip specific controllers, such that for each flash chip used, a separate controller compatible with the flash chip must be employed on the flash chip. Thus, unlike claim 16, where programmable flash

medium logic may be programmed by a user to interact with a flash memory medium, under Ban a new controller must be chosen to interact with each new flash chip.

In rejecting claim 16, the Office relies on the same bases used in the rejection of claims 1 and 7 -- namely Fig.1; claim 2; the Abstract; Col. 2, lines 36-48; Col. 4, lines 33-39 and 61-65; and Col. 3, line 49 – Col. 4, line 13 of Ban. (*Office Action*, Page 5). However, as noted above, Ban fails to disclose or show both "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium" and "wherein the flash memory driver is flash memory medium agnostic".

Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 16 be withdrawn.

Dependent claims 17 and 22 are allowable at the least by virtue of their dependency on base claim 16, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 17 and 22 be withdrawn.

Independent claim 23 recites:

> A processing device that uses a flash memory medium for storage of data, comprising:
>
> a file system, configured to control data storage for the processing device;
>
> flash media logic, configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable entry points that can be implemented by a user to interface with any type of flash memory medium selected; and
>
> flash abstraction logic, configured to maintain flash memory requirements that are necessary to operate the flash memory medium.

Ban fails to disclose the processing device of claim 23. As noted above, under Ban a separate compatible controller must also be used for each flash chip employed. This is different than a flash media logic including "a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" disclosed in claim 23. One difference lies in the fact that the flash media logic of claim 23 may easily be used with multiple, different flash media. In contrast, under Ban, multiple controllers would be needed to interface with multiple, different flash chips.

In rejecting claim 23, the Office relies on Ban, Col. 2, lines 17-23 and 36-48; Col. 3, lines 15-24; and Fig 1. (*Office Action*, Page 4). Applicant respectfully disagrees. As noted above, Ban discloses using different controllers for different flash chips, wherein each controller is located on the flash chip it serves. Thus, a flash medium logic that can interface with several types of flash memory media makes no sense under Ban.

In addition, no mention is made in Ban regarding a set of *programmable entry points* on the flash medium logic that can be implemented by a user to interface with the type of flash memory medium selected, such as is recited in claim 23.

In rejecting this portion of claim 23, the Office relies on Col. 3, lines 15-24. (*Office Action*, Page 4). Applicant respectfully disagrees, as this passage has nothing to do with programmable entry points, and instead discloses a command register on a controller into which a command from the CPU is written before the command is translated by the controller to a command particular to the flash unit to which the controller is attached. Thus, "*programmable entry points* that can be

implemented by a user to interface with any type of flash memory medium selected" as recited in claim 23 is not disclosed in Ban.

Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 23 be withdrawn.

Dependent claims 24-32 are allowable at the least by virtue of their dependency on base claim 23, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 24-32 be withdrawn.

Independent claim 33 recites:

> In a processing device that uses a flash memory medium for storage of data, a method for driving the flash memory medium, comprising:
>
> managing rules associated with operating the flash memory medium in a flash abstraction logic; and
>
> issuing physical sector commands directly to the flash memory medium from a flash medium logic;
>
> wherein the method is flash memory medium agnostic.

Ban fails to disclose the processing device of claim 33. In particular, as noted above, under Ban a separate, unique controller must be used for each flash chip employed. This is different than "wherein the method is flash memory medium agnostic" disclosed in claim 33. The difference lies in the fact that the flash media logic of claim 33 may easily be used with multiple, different flash media. In contrast, under Ban, multiple controllers would be needed to interface with multiple, different flash chips.

The Office argues that the claimed method for driving the flash memory medium is shown in Fig.1; claim 2; the Abstract; Col. 2, lines 36-48; claim 7; Col.

3, lines 19-24 of Ban; Col. 4, lines 33-29 and 61-65; and Col. 3, line 49-Col. 4, line 13 of Ban. (*Office Action*, Page 6). Applicant respectfully disagrees. As noted above, under Ban a unique controller must be used for each flash chip, with each controller being located on the flash chip it serves. Thus, a flash memory medium agnostic method as recited in claim 33 makes no sense under Ban. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 33 be withdrawn.

Dependent claims 37 and 39-41 are allowable at the least by virtue of their dependency on base claim 33, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 37 and 39-41 be withdrawn.

Independent claim 42 recites:

> A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to provide an interface between a file system, selected from one of a plurality of different file systems, and a flash memory medium, selected from one of a plurality of different flash memory media, wherein the flash driver is located remote from the flash memory medium.

Ban fails to disclose the computer readable medium for a flash driver of claim 42. As discussed above, under Ban a separate, unique controller must be used for each flash chip employed, with each controller being located on the flash chip it serves. This is different than "the flash driver to provide an interface between a file system, selected from one of a plurality of different file systems, and a flash memory medium, selected from one of a plurality of different flash memory

media" and "the flash driver is located remote from the flash memory medium" disclosed in claim 42.

In rejecting claim 42, the Office relies on the same bases used to reject claim 1 -- Fig. 1; claim 2; the Abstract; and Col. 2, lines 36-48 of Ban. (*Office Action*, Page 5). Applicant respectfully disagrees. As discussed in more detail above, these passages disclose placing separate controllers on each flash chip in a flash array in order to interface with a CPU. Thus no one controller can interface with "a flash memory medium, selected from one of a plurality of different flash memory media" as recited in claim 42. Instead, under Ban, a plurality of controllers would be required to fulfill such a function. Moreover, none of the controllers disclosed in Ban are located remote from the flash memory medium. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 42 be withdrawn.

Independent claim 43 recites:

> A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:
>
> provide an interface between a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media; and
>
> manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic;
>
> wherein the flash driver is flash memory medium agnostic.

Ban fails to disclose the computer-readable medium for a flash driver of claim 43. Similar to claim 42 above, under Ban, the responsibility for conforming

to the particular requirements of each flash chip is given to a controller installed on each flash chip. Thus the controllers used under Ban are flash chip specific, and can provide an interface for only one chip. Therefore, a single controller under Ban cannot provide an interface between "one of a plurality of different flash memory media" as disclosed in claim 43. Rather, under Ban, in order to provide an interface with more than one different flash chip, an equivalent number of controllers would be needed, with a unique controller being located on each flash chip. Therefore Ban does not disclose "provide an interface between a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media" as recited in claim 43.

Moreover, since the controllers disclosed in Ban are flash chip specific, it would take a plurality of controllers to manage characteristics common to a plurality of flash chips. Therefore, Ban does not disclose a flash driver which can "manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic" as is recited in claim 43. Rather, under Ban a plurality of controllers having flash abstraction logic would be required to fulfill this function.

Additionally, since each controller is located on a corresponding flash chip, and exclusively serves only that flash chip, "wherein the flash driver is flash memory medium agnostic" makes no sense under Ban.

The Office argues that the same passages cited with regard to claim 42 above disclose the claimed computer-readable medium claimed in claim 43. (*Office Action*, Page 5). Applicant respectfully disagrees. As noted above, these passages disclose placing separate controllers on each flash chip in an array in

order to interface with a CPU. Thus, under Ban no one controller can interface with a flash memory medium, selected from one of a plurality of different flash memory media, and no one controller can manage a set of characteristics common to a plurality of different flash memory media at a flash abstraction logic. Nor is any one controller flash memory medium agnostic.

Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 43 be withdrawn.

Independent claim 44 recites:

> A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:
>
> provide an interface between a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media;
>
> manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic; and
>
> provide programmable entry points that can be optionally selected by a user to interface with the type of flash memory medium selected;
>
> wherein the flash driver is located remote from the flash memory medium and the flash driver is flash memory medium agnostic.

Ban fails to disclose the computer-readable medium for a flash driver of claim 44. As discussed above, under Ban a single controller cannot provide an interface between "a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media". Moreover, it also follows that a controller under Ban

cannot "manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic". To achieve this sort of functionality, Ban would require a plurality of controllers rather that the single flash driver recited in claim 44.

In addition, since a controller under Ban is configured to interface with a particular flash chip -- and is even located on a particular flash chip -- a controller under Ban could not be used to "provide programmable entry points that can be optionally selected by a user to interface with the type of flash memory medium selected". This would imply that a controller disclosed in Ban could work with several different flash chips, which it can't. Moreover, there is no disclosure in Ban which mentions "programmable entry points that can be optionally selected by a user". Rather, under Ban the user is limited to the use of a specific controller adapted to operate with a specific flash chip. No other choice is possible.

Additionally, since each controller is uniquely configured for the flash chip on which it is located, a "flash driver is located remote from the flash memory medium and the flash driver is flash memory medium agnostic" makes no sense under Ban.

The Office rejects claim 43 on the same bases used in rejecting claim 1 – Fig.1, and Col. 2, lines 33-39 and 61-65, Col. 4, lines 33-39, claim 2, and the Abstract (*Office Action*, Pages 2, 3 and 5). Applicant respectfully disagrees. Ban discloses only controllers that are configured for one specific type of flash chip. Thus the versatility recited in claim 44 above would be impossible under Ban. Moreover, nowhere does Ban disclose "programmable entry points that can be optionally selected by a user to interface with the type of flash memory medium selected". Furthermore, since each controller under Ban is uniquely configured for

the flash chip on which it is located, a "flash driver is located remote from the flash memory medium and the flash driver is flash memory medium agnostic" makes no sense under Ban. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 44 be withdrawn.

35 U.S.C. §103(a)

The remaining claims are rejected under a set of §103 rejections, all of which rely on Ban as the primary reference. Moreover, all of these claims depend from base claims addressed above.

Ban +Bruce

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Bruce. Applicant respectfully traverses the rejection.

Claims 2, 12, 20, 27 and 35 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. The combination of Ban and Bruce fails to teach or suggest the features of these base claims from which the cited claims depend. Ban is primarily cited as teaching the base features, and Bruce is cited as teaching the use of a unified remapping and wear leveling table to overcome the disadvantages of the larger granularity of block remapping.

With respect to **dependent claim 2,** neither reference discloses, "flash media logic configured to interact with different types of the flash memory media" or "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on

the type of the flash memory media". Instead, as discussed above, Ban teaches that the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip. Thus interacting with different types of flash memory media would require several controllers rather that the single flash memory driver recited in claim 1 from which claim 2 depends.

Bruce offers no missing teaching. Accordingly, the combination of Ban and Bruce fails to teach or suggest the device of claim 2. Applicant respectfully requests that the §103 rejection of claim 2 be withdrawn.

With respect to **dependant claim 12,** neither reference discloses "flash abstraction logic, interposed between a file system and a flash memory medium, configured to: (a) map a logical sector status from the file system to a physical sector status of the flash memory medium" as recited by claim 9 from which claim 12 depends. Rather Ban teaches the opposite of this by disclosing that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, under Ban the CPU, rather than the flash driver, coordinates and organizes all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Bruce offers no missing teaching. Accordingly, the combination of Ban and Bruce fails to teach or suggest the device of claim 12. Applicant respectfully requests that the §103 rejection of claim 12 be withdrawn.

With respect to **dependant claim 20**, for the reasons just given, neither Ban nor Bruce teaches or suggests "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium". Accordingly,

the combination of Ban and Bruce fails to teach or suggest the device of claim 20. Applicant respectfully requests that the §103 rejection of claim 20 be withdrawn.

With respect to **dependant claim 27,** neither Ban nor Bruce teaches or suggests "a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" as recited in claim 23 from which claim 27 depends. Ban teaches that a separate compatible controller must be used for each flash chip employed, with each controller being attached to the flash chip it serves. This teaches away from the processing device of claim 27 which may be used with multiple, different flash chips. In contrast, under Ban, multiple controllers would be needed to interface with multiple flash chips.

Again, Bruce offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claim 27 be withdrawn.

With respect to **dependant claim 35,** neither reference discloses, teaches or suggests "issuing physical sector commands directly to the flash memory medium from a flash medium logic" as recited in claim 33 from which claim 35 depends. Ban teaches that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, Ban teaches away from claim 33 and claim 35, which depends from claim 33, by specifying that the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Bruce offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claim 35 be withdrawn.

Ban + Martwick

Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Martwick. Applicant respectfully traverses the rejection.

Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. The combination of Ban and Martwick fails to teach or suggest the features of the base claims from which the cited claims depend. Ban is primarily cited as teaching the base features, and Martwick is cited as teaching a method for updating flash blocks so that data integrity gets maintained and data can be recovered upon a power failure.

Dependent claims 3 and 4 depend from claim 1, and hence include the features therein. Neither Ban nor Martwick disclose, "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1. As noted above, Ban specifically teaches giving the responsibility for conforming to the particular requirements of a flash chip to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips. Therefore, each time a new flash chip is used, a new controller that is compatible with the new flash chip must be located on the flash chip.

In addition, neither reference discloses, teaches or suggests "flash media logic configured to interact with different types of the flash memory media" or "wherein the flash abstraction logic invokes the flash media logic to perform

memory operations that are potentially performed in different ways depending on the type of the flash memory media". Instead, Ban teaches that the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip. Thus interacting with different types of flash memory media would require several controllers rather that the single flash memory driver recited in claim 1 from which claims 3 and 4 depend.

Martwick fails to add any relevant teaching with respect to these features. Accordingly, the combination of Ban and Martwick fails to teach or suggest the device of claims 3 and 4. Applicant respectfully requests that the §103 rejection of claims 3 and 4 be withdrawn.

Similarly **dependant claims 13 and 14** depend from base claim 9 and thus include the features therein. Ban fails to teach or suggest "flash abstraction logic, interposed between a file system and a flash memory medium, configured to: (a) map a logical sector status from the file system to a physical sector status of the flash memory medium" as recited in claim 9 from which claims 13 and 14 depend. As previously discussed, Ban teaches away from this by disclosing that during a read/write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, under Ban the CPU, rather than the flash driver, coordinates and organizes all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Martwick offers no missing teaching. Accordingly, the combination of Ban and Martwick fails to teach or suggest the device of claims 13 and 14. Applicant respectfully requests that the §103 rejection of claims 13 and 14 be withdrawn.

Dependant claims 19 and 21 depend from base claim 16 and hence include the features therein. For the reasons just given, neither reference teaches or suggests "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium". Accordingly, the combination of Ban and Martwick fails to teach or suggest the devices of claims 19 and 21. Applicant respectfully requests that the §103 rejection of claims 19 and 21 be withdrawn.

Dependant claims 26 and 28 depend from base claim 23 and hence include the features therein. Neither reference teaches or suggests "a set of programmable entry points that can be implemented by a user to interface with any type of flash memory medium selected" as recited in claim 23 from which claims 26 and 28 depend. Instead, Ban teaches that a separate compatible controller must be used for each flash chip employed. This teaches away from the processing device of claims 26 and 28, which may be used with multiple, different flash chips. In contrast, under Ban multiple controllers would be needed to interface with multiple flash chips. Moreover, Ban fails to teach a set of programmable entry points as recited in claim 23.

Again, Martwick offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claims 26 and 28 be withdrawn.

Similarly, **dependant claims 34 and 36** depend from base claim 33 and hence include the features therein. Neither reference discloses, teaches or suggests "issuing physical sector commands directly to the flash memory medium from a flash medium logic" as recited in claim 33 from which claims 33 and 36 depend. Instead, Ban teaches that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, Ban teaches away

from claims 33, 34 and 36 by specifying that the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Martwick offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claims 34 and 36 be withdrawn.

Ban + Hall

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall. Applicant respectfully traverses the rejection.

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. The combination of Ban and Hall fails to teach or suggest the features of the base claims from which the cited claims depend. Ban is primarily cited as teaching the base features, and Hall is cited as teaching a flash memory medium agnostic flash driver, a flash driver located remote from the flash memory medium, and flash media logic that is configured to interact with different types of flash memory media.

As noted above, Ban fails to teach several elements in claims 1, 9, 16, 23, and 33, including a flash memory driver which is memory medium agnostic, a flash driver located remote from the flash memory medium, and a flash medium logic comprising a set of programmable entry points that can be implemented by a user to interface with any type of flash memory medium selected. Moreover, as also discussed above, Ban teaches shifting the responsibility for conforming to the

particular requirements of a flash chip from a standardized driver installed on a CPU to a controller *installed on a flash unit*. According to Ban, the standardized driver on the CPU sends out generic commands (read, write, erase and identify) in a uniform, standardized format which are received via a command register and are translated by the standardized controller *on the flash unit* (through a translating apparatus) into commands specific to the type of flash chip on which the controller is installed. Thus, when a flash array including multiple flash chips is used, each flash chip must be provided with a standardized controller customized to interact with only the particular chip *to which it is attached*. Consequently, in order for the CPU to communicate with several different types of flash chips, a corresponding number of different, uniquely customized controllers must be utilized on each flash chip.

In contrast, Hall teaches sending command-type signals from a processor directly to a flash memory, with the signals being tailored by the processor to be compatible with the specific type of flash memory. (Col. 1, line 61- Col 2, line 16; and Col. 3, lines 51-59). This is the exact opposite of the behavior of the CPU taught in Ban, which sends standardized signals *to be later* translated by controllers located on flash chips. Thus, there is no motivation to combine Ban with Hall, and in fact, Ban teaches away from combination with Hall by contradicting the teachings of Hall. Accordingly, Hall may not be properly combined with Ban. On this basis alone, Applicant respectfully requests that the §103 rejection of claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 be withdrawn.

Moreover, both Ban and Hall, either alone or in combination, fail to disclose, teach or suggest a flash medium logic comprising a set of programmable

entry points that can be implemented by a user to interface with any type of flash memory medium selected. Thus, even if Ban and Hall could be combined, they would fail to teach or suggest all of the elements found in claim 22, claim 23 (from which claims 24-32 depend), and claims 30, 38, 39 and 44. On this basis alone, Applicant respectfully requests that the §103 rejection of claims 22-25, 29, 31-32, 39, and 44 be withdrawn.

Ban + Hall + Bruce

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall, and further in view of Bruce. Applicant respectfully traverses the rejection.

Claims 2, 12, 20, 27 and 35 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. As noted above, there is no motivation to combine Ban with Hall, and in fact, Ban teaches away from combination with Hall by contradicting the teachings of Hall. Accordingly, Hall may not be properly combined with Ban. And, as also discussed above, Ban fails to disclose, teach or suggest the elements of claims 1, 9, 16, 23, and 33, and Bruce fails to add any of Ban's missing teachings. On this basis alone, Applicant respectfully requests that the §103 rejection of claims 2, 12, 20, 27 and 35 be withdrawn.

Moreover, Ban, Hall, and Bruce, either alone or in combination, fail to disclose, teach or suggest a flash medium logic comprising a set of programmable entry points that can be implemented by a user to interface with any type of flash memory medium selected. Thus, even if Ban and Hall could be combined, they, in combination with Bruce, would fail to teach or suggest all of the elements found in

claims 27. On this basis alone, Applicant respectfully requests that the §103 rejection of claim 27 be withdrawn.

Ban + Hall + Martwick

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall, and further in view of Martwick. Applicant respectfully traverses the rejection.

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. As noted above, there is no motivation to combine Ban with Hall, and in fact, Ban teaches away from combination with Hall by contradicting the teachings of Hall. Accordingly, Hall may not be properly combined with Ban. Moreover, as also discussed above, Ban fails to disclose, teach or suggest the elements of claims 1, 9, 16, 23, and 33, and Martwick fails to add any of Ban's missing teachings. On this basis alone, Applicant respectfully requests that the §103 rejection of claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 be withdrawn.

Moreover, Ban, Hall, and Martwick, either alone or in combination, fail to disclose, teach or suggest a flash medium logic comprising a set of programmable entry points that can be implemented by a user to interface with any type of flash memory medium selected. Thus, even if Ban and Hall could be combined, they, in combination with Martwick, would fail to teach or suggest all of the elements found in claims 26 and 28. On this basis alone, Applicant respectfully requests that the §103 rejection of claims 26 and 28 be withdrawn.

CONCLUSION

All pending claims 1-44 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

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By: Jim Patterson

Jim Patterson
Reg. No. 52,103
(509) 324-9256 ext. 247